

WT0132P4-A1 Datasheet



Version 2.4

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Revision History

| Version | Date | Developed/ Changed Content | Modifier By | Auditor |
|---------|-----------|--|-------------|---------|
| V1.0 | 2024-9-12 | First Creation | Pail | Louie |
| V1.1 | 2025-2-06 | 1.WT0132P4-A1 pin layout & description, modify pin 32 description. 2.Increase the cross-section of WT0132P4-A1 core board size. | Pail | Louie |
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| V2.1 | 2025-4-09 | 1.Make additional explanations to some of the pins in 3.2Pin Description 2.Errata to 4.3 Recommended Working Conditions 3.Update dimension figure of WT0132P4-A1 | Pail | Louie |
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| V2.4 | 2025-7-28 | 1.Modify the pin layout diagram in 3.1 Pin Layout. | Pail | Louie |

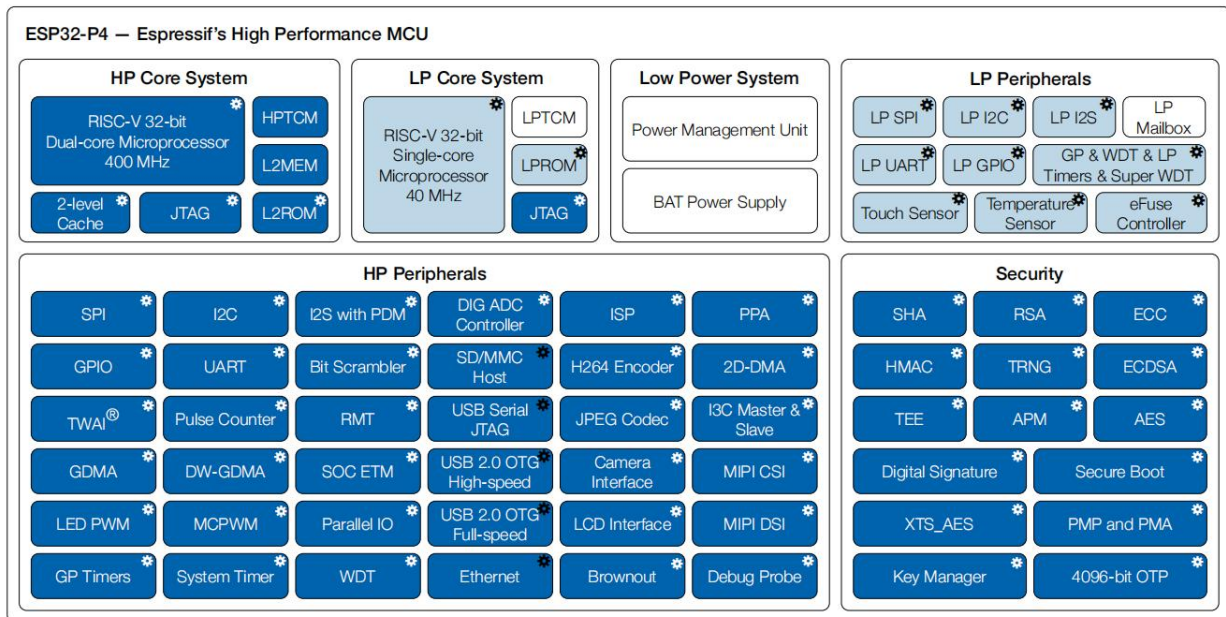
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1. Overview

1.1. Products Introduction

WT0132P4-A1 is an integrated NOR FLASH small core board based on Espressif ESP32-P4 chip designed by Wireless-Tag Technology Co., Limited. The core processor chip, ESP32-P4, can be stacked with 16MB or 32MB PSRAM in the package, and contains a high-performance (HP) system and a low-power (LP) system; the HP system adopts a RISC-V dual-core processor with a main frequency up to 360MHz, and contains a JPEG encoder/decoder, pixel-processing gas pedal, H.264 video encoder, and a MIPI interface; it has powerful image and voice processing capabilities. The HP system uses a RISC-V dual-core processor with up to 360MHz, including a JPEG coder/decoder, pixel processing accelerator, H.264 video encoder, and MIPI interface.



Modules having power in specific power modes:



Figure 1: Main Chip Architecture Diagram

The WT0132P4-A1 series is available in two sizes, see the table below for more information.

WT0132P4-A1 Series Model Number Comparison

| Part Number | Flash | PsrAm | Module Size (mm) |
|--------------------|-------|-------|------------------|
| WT0132P4-A1-N16R16 | 16MB | 16MB | 25.00*20.00 |
| WT0132P4-A1-N16R32 | 16MB | 32MB | 25.00*20.00 |

1.2.Product Features

- Dual-core 360 MHz high-frequency CPU
- 16 MB Flash and 16/32 MB Psram
- ESP32-P4 chip with full pinout
- Supports multiple multimedia interfaces
- Core board size is small, easy to hardware design
- Development materials are complete

1.3.Product Pictures



Figure 2:WT0132P4-A1(front)



Figure 3:WT0132P4-A1 (back)



Figure 4:WT0132P4-A1(front)



Figure 5:WT0132P4-A1(back)

1.4.Application Scenarios

- Smart Home
- Industrial Automation
- Consumer Electronics
- HMI Human Machine Interaction
- Electronic Robotics
- Camera Video Streaming
- USB Devices

2. Product Specification

2.1.Block Diagram

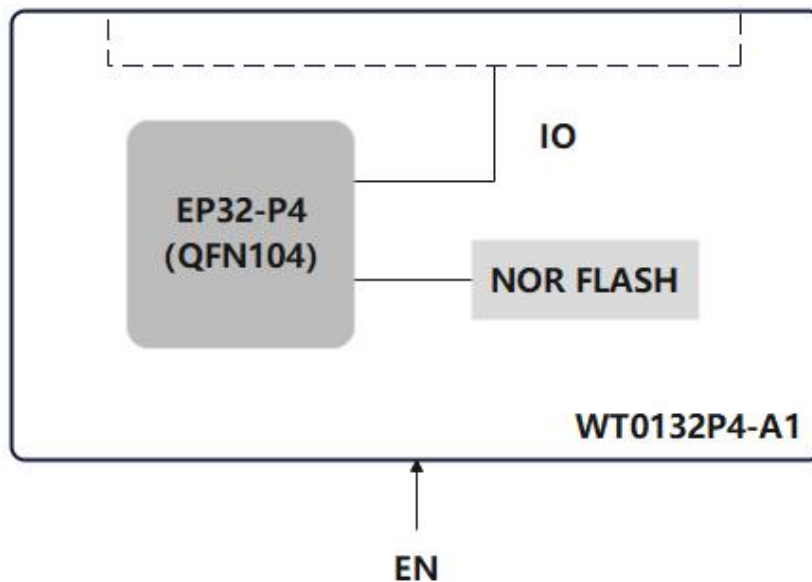


Figure 6: Block diagram of WT0132P4-A1

2.2.Hardware Parameters

| | | |
|--------|----------------|---------------------------------------|
| CPU | CPU | ESP32-P4 |
| | Core | 32-bit RISC-V dual-core |
| | Main Frequency | 360 MHz (HP Core) 40 MHz (LP Core) |
| Memory | ROM | 128 KB HP ROM |
| | | 16 KB LP ROM |



| | | |
|-----------------------------|--|-----------------|
| | SRAM | 768 KB HP L2MEM |
| | | 32 KB LP SRAM |
| | Flash | 16 MB |
| Peripheral Interface | GPIO | 55 |
| | SPI | 2 |
| | LP SPI | 1 |
| | UART | 5 |
| | LP UART | 1 |
| | I3C | 1 |
| | I2C | 2 |
| | LP I2C | 1 |
| | I2S | 3 |
| | LP I2S | 1 |
| | USB JTAG | 1 |
| | SDIO | 1 |
| | LED PWM | 1 |
| | MCPWM | 2 |
| | TWAI®Controller (compatible with ISO 11898-1) | 3 |
| | High-Speed USB 2.0 OTG | 1 |
| | Full-Speed USB 2.0 OTG | 1 |
| | 100 Mbit Ethernet | 1 |
| | MIPI CSI-2 | 1 |
| | MIPI DSI | 1 |
| | Parallel IO interface | 1 |
| | 12-bit multi-channel ADC | 2 |
| | Temperature sensor | 1 |
| | Touch sensor | 1 |
| | Analog voltage comparator | 1 |

| | | |
|---|--------------------|---|
| | Brown-out detector | 1 |
| Image and Voice Processing Functionality | JPEG Codec | 1 |
| | PPA | 1 |
| | ISP | 1 |
| | H264 encoder | 1 |

3. Pin Definitions

3.1.Pin Layout

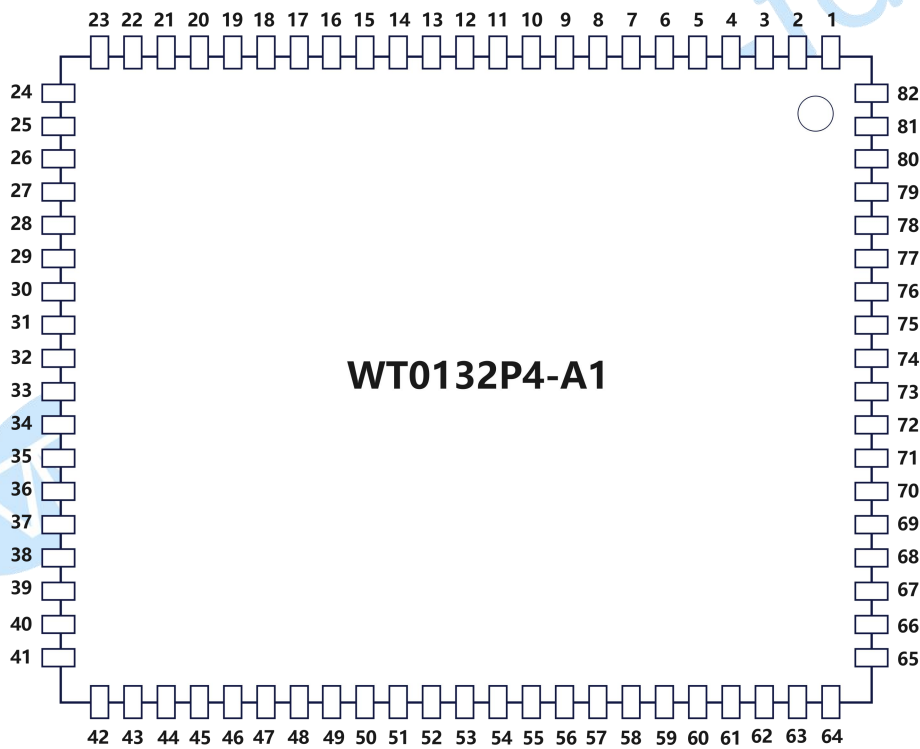


Figure 7:WT0132P4-A1 Pin Layout

3.2.Pin Description

Pin Definitions

| No. | Name | Function |
|-----|------------|---------------------|
| 1 | GND | GROUND |
| 2 | DSI_DATAP1 | MIPI DSI PHY DATAP1 |
| 3 | DSI_DATAN1 | MIPI DSI PHY DATAN1 |
| 4 | DSI_CLKN | MIPI DSI PHY CLKN |
| 5 | DSI_CLKP | MIPI DSI PHY CLKP |



| | | |
|----|------------|--|
| 6 | DSI_DATAP0 | MIPI DSI PHY DATAP0 |
| 7 | DSI_DATAN0 | MIPI DSI PHY DATAN0 |
| 8 | GND | GROUND |
| 9 | CSI_DATAN0 | MIPI CSI PHY DATAN0 |
| 10 | CSI_DATAP0 | MIPI CSI PHY DATAP0 |
| 11 | CSI_CLKP | MIPI CSI PHY CLKP |
| 12 | CSI_CLKN | MIPI CSI PHY CLKN |
| 13 | CSI_DATAN1 | MIPI CSI PHY DATAN1 |
| 14 | CSI_DATAP1 | MIPI CSI PHY DATAP1 |
| 15 | GND | GROUND |
| 16 | USB_DM | USB2 OTG PHY DM |
| 17 | USB_DP | USB2 OTG PHY DP |
| 18 | GND | GROUND |
| 19 | GPIO24 | GPIO24, USB1P1_N0 |
| 20 | GPIO25 | GPIO25, USB1P1_P0 |
| 21 | GND | GROUND |
| 22 | GPIO26 | GPIO26, USB1P1_N1 |
| 23 | GPIO27 | GPIO27, USB1P1_P1 |
| 24 | GPIO28 | GPIO28, GPSPI SPI2 CS, EMAC PHY RXDV, DBG_PSRAM_D |
| 25 | GPIO29 | GPIO29, GPSPI SPI2 D, EMAC PHY RXD0, DBG_PSRAM_Q |
| 26 | GPIO30 | GPIO30, GPSPI SPI2 CK, EMAC PHY RXD1, DBG_PSRAM_WP |
| 27 | GPIO31 | GPIO31, GPSPI SPI2 Q, EMAC PHY RXER, DBG_PSRAM_HOLD |
| 28 | GPIO32 | GPIO32, I3CMST_SCL, GPSPI SPI2 HOLD. EMAC RMII CLK, DBG_PSRAM_DQ4 |
| 29 | GPIO33 | gpio33, i3cmst_sda, gpspi spi2 wp. |

| | | |
|----|-------------|---|
| | | EMAC PHY TXEN, DBG_PSRAM_DQ5 |
| 30 | GPIO34 | GPIO34, GPSPI SPI2 IO4, EMAC PHY TXD0, DBG_PSRAM_DQ6 |
| 31 | GPIO35 | GPIO35, GPSPI SPI2 IO5, EMAC PHY TXD1, DBG_PSRAM_DQ7 (IO35 pulls down into download mode) |
| 32 | ESP_LDO_VO4 | Output POWER (Output voltage range 0.5~2.7V or 3.3V, maximum output current 0.2A) |
| 33 | GPIO36 | GPIO36, GPSPI SPI2 IO6, EMAC PHY TXER, DBG_PSRAM_DQS0 (Default IO35, 36 pull-up to enter SPI Boot mode) |
| 34 | GPIO37 | GPIO37, UART0_TXD, GPSPI SPI2 IO7 (Download port) |
| 35 | GPIO38 | GPIO38, UART0_RXD, GPSPI SPI2 DQS (Download port) |
| 36 | GPIO39 | GPIO39, SD1_CDATA0_PAD, REF_50M_CLK_PAD |
| 37 | GPIO40 | GPIO40, SD1_CDATA1_PAD, GMAC_PHY_TXEN_PAD |
| 38 | GPIO41 | GPIO41, SD1_CDATA2_PAD, GMAC_PHY_TXD0_PAD |
| 39 | GPIO42 | GPIO42, SD1_CDATA3_PAD, GMAC_PHY_TXD1_PAD |
| 40 | GPIO43 | GPIO43, SD1_CCLK_PAD, GMAC_PHY_TXER_PAD |
| 41 | VCC | POWER (5V input for core board power supply) |
| 42 | GND | GROUND |
| 43 | GPIO44 | GPIO44, SD1_CCMD_PAD, GMAC_RMII_CLK_PAD |
| 44 | GPIO45 | GPIO45, SD1_CDATA4_PAD, GMAC_PHY_RXDV_PAD |
| 45 | GPIO46 | GPIO46, SD1_CDATA5_PAD, GMAC_PHY_RXD0_PAD |
| 46 | GPIO47 | GPIO47, SD1_CDATA6_PAD, GMAC_PHY_RXD1_PAD |
| 47 | GPIO48 | GPIO48, SD1_CDATA7_PAD, GMAC_PHY_RXER_PAD |
| 48 | GPIO49 | GPIO49, GMAC_PHY_TXEN_PAD, ADC2_CHANNEL2 |
| 49 | GPIO50 | GPIO50, GMAC_RMII_CLK_PAD, ADC2_CHANNEL3 |

| | | |
|----|--------|--|
| 50 | GPIO51 | GPIO51, GMAC_PHY_RXDV_PAD, ADC2_CHANNEL4, ANA_COMP0 |
| 51 | GPIO52 | GPIO52, GMAC_PHY_RXD0_PAD, ADC2_CHANNEL5, ANA_COMP0 |
| 52 | GPIO53 | GPIO53, GMAC_PHY_RXD1_PAD, ADC2_CHANNEL6, ANA_COMP1 |
| 53 | GND | GROUND |
| 54 | GPIO54 | GPIO54, GMAC_PHY_RXER_PAD, ADC2_CHANNEL7, ANA_COMP1 |
| 55 | GPIO2 | GPIO2, MTCK, LP_GPIO 2, TOUCH_CHANNEL0 |
| 56 | GPIO3 | GPIO3, MTDI, LP_GPIO 3, TOUCH_CHANNEL1 |
| 57 | GPIO4 | GPIO4, MTMS, LP_GPIO4, TOUCH_CHANNEL2 |
| 58 | GPIO5 | GPIO5, MTDO, LP_GPIO5, TOUCH_CHANNEL3 |
| 59 | GPIO6 | GPIO6, SPI2_HOLD_PAD, LP_GPIO6, TOUCH_CHANNEL4 |
| 60 | GPIO7 | GPIO7, SPI2_CS_PAD, LP_GPIO7, TOUCH_CHANNEL5 |
| 61 | GPIO8 | GPIO8, UART0_RTS_PAD, SPI2_D_PAD , LP_GPIO8, TOUCH_CHANNEL6 |
| 62 | GPIO9 | GPIO9, UART0_CTS_PAD, SPI2_CK_PAD, LP_GPIO9, TOUCH_CHANNEL7 |
| 63 | GPIO10 | GPIO10, UART1_TXD_PAD, SPI2_Q_PAD, LP_GPIO10, TOUCH_CHANNEL8 |
| 64 | GND | GROUND |
| 65 | GPIO11 | GPIO11, UART1_RXD_PAD, SPI2_WP_PAD, LP_GPIO11, TOUCH_CHANNEL9 |
| 66 | GPIO12 | GPIO12, UART1_RTS_PAD , LP_GPIO12, TOUCH_CHANNEL10 |
| 67 | GPIO13 | GPIO13, UART1_CTS_PAD, LP_GPIO13, TOUCH_CHANNEL11 |
| 68 | GPIO14 | GPIO14, LP_GPIO14, LP_UART_TXD_PAD, |

| | | |
|----|---------|--|
| | | TOUCH_CHANNEL12 |
| 69 | GPIO15 | GPIO15, LP_GPIO15, LP_UART_RXD_PAD, TOUCH_CHANNEL13 |
| 70 | CHIP_PU | Enable P4 chip (internal 10K pull-up) |
| 71 | GPIO0 | GPIO0, LP_GPIO0, XTAL_32K_N |
| 72 | GPIO 1 | GPIO1, LP_GPIO1, XTAL_32K_P |
| 73 | GND | GROUND |
| 74 | GPIO16 | GPIO16, ADC1_CHANNEL0 |
| 75 | GPIO17 | GPIO17, ADC1_CHANNEL1 |
| 76 | GPIO18 | GPIO18, ADC1_CHANNEL2 |
| 77 | GPIO19 | GPIO19, ADC1_CHANNEL3 |
| 78 | GPIO20 | GPIO20, ADC1_CHANNEL4 |
| 79 | GPIO21 | GPIO21, ADC1_CHANNEL5 |
| 80 | GPIO22 | GPIO22, ADC1_CHANNEL6 |
| 81 | GPIO23 | GPIO23, ADC1_CHANNEL7, REF_50M_CLK_PAD |
| 82 | GND | GROUND |

3.3.Startup Item Configuration

3.3.1. Strapping Pins

The chip allows for configuring the following boot parameters through strapping pins and eFuse bits at power-up or a hardware reset, without microcontroller interaction.

- **Chip Boot Mode**
 - Strapping pin: GPIO35, GPIO36, GPIO37 and GPIO38
- **ROM Message Printing**
 - Strapping pin: GPIO36
 - eFuse bit: EFUSE_UART_PRINT_CONTROL
- **JTAG Signal Source**
 - Strapping pin: GPIO34

– eFuse bit: EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG and EFUSE_JTAG_SEL_ENABLE

The default values of all the above eFuse bits are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once an eFuse bit is programmed to 1, it can never be reverted to 0.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Default Configuration of Strapping Pin

| Strapping Pin | Default Configuration | Value |
|---------------|-----------------------|-------|
| GPIO34 | Floating | - |
| GPIO35 | Weak pull-up | 1 |
| GPIO36 | Floating | - |
| GPIO37 | Floating | - |
| GPIO38 | Floating | - |

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistors. If the ESP32-P4 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

3.3.2. Chip Boot Mode Control

GPIO35 ~ GPIO38 control the boot mode after the reset is released.

| Boot Mode | GPIO35 | GPIO36 | GPIO37 | GPIO38 |
|-----------|--------|-----------|-----------|-----------|
| SPI Boot* | 1* | Any value | Any value | Any value |

| | | | | |
|---------------------|---|---|-----------|-----------|
| Joint Download Boot | 0 | 1 | Any value | Any value |
|---------------------|---|---|-----------|-----------|

*marks the default value and configuration.

Joint Download Boot mode supports the following download methods:

- USB Download Boot:
 - USB-Serial-JTAG Download Boot
 - USB 2.0 OTG Download Boot
- UART Download Boot
- SPI Slave Download Boot

3.3.3. ROM Messages Printing Control

During the boot process, the messages by the ROM code can be printed to:

- **(Default) UART0 and USB Serial/JTAG controller**
- USB Serial/JTAG controller
- UART0

EFUSE_UART_PRINT_CONTROL and GPIO36 control ROM messages printing to UART0 as shown in Table.

| UART0 Code Printing | EFUSE_UART_PRINT_CONTROL | GPIO36 |
|---------------------|--------------------------|---------|
| Enabled* | 0* | Ignored |
| | 1 | 0 |
| | 2 | 1 |
| Disabled | 1 | 1 |
| | 2 | 0 |
| | 3 | Ignored |

*marks the default value and configuration.

EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT controls the printing to USB Serial/JTAG controller as shown in Table.

| USB Serial/JTAG ROM Code Printing | EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT |
|-----------------------------------|-------------------------------------|
| Enabled* | 0* |
| Disabled | 1 |

*marks the default value and configuration.

4. Electrical Characteristics

4.1. Absolute Maximum Limit Value

Exceeding the absolute maximum ratings may result in permanent damage to the device. This is an emphasized rating only and does not address the functional operation of the device under these or other conditions beyond those indicated in these specifications. Prolonged exposure to absolute maximum rating conditions may affect module reliability.

4.2. Power Consumption Characteristics

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4.3. Recommended Working Conditions

| Parameter | Description | Min | Typ | Max | Unit |
|------------------|---|-----|-----|-----|------|
| VCC | Power pin voltage | 4.8 | 5 | 5.5 | V |
| I _{VCC} | Supply current from external power supply | - | 1 | - | A |
| T _A | Operating Temperature | -40 | - | 85 | °C |

5. WT0132P4-A1 Schematic

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Figure 8: WT0132P4-A1 Schematic

6. WT0132P4-A1 Dimensions

The following figure shows the top view and front view of WT0132P4-A1 with a tolerance of ± 0.2 mm.

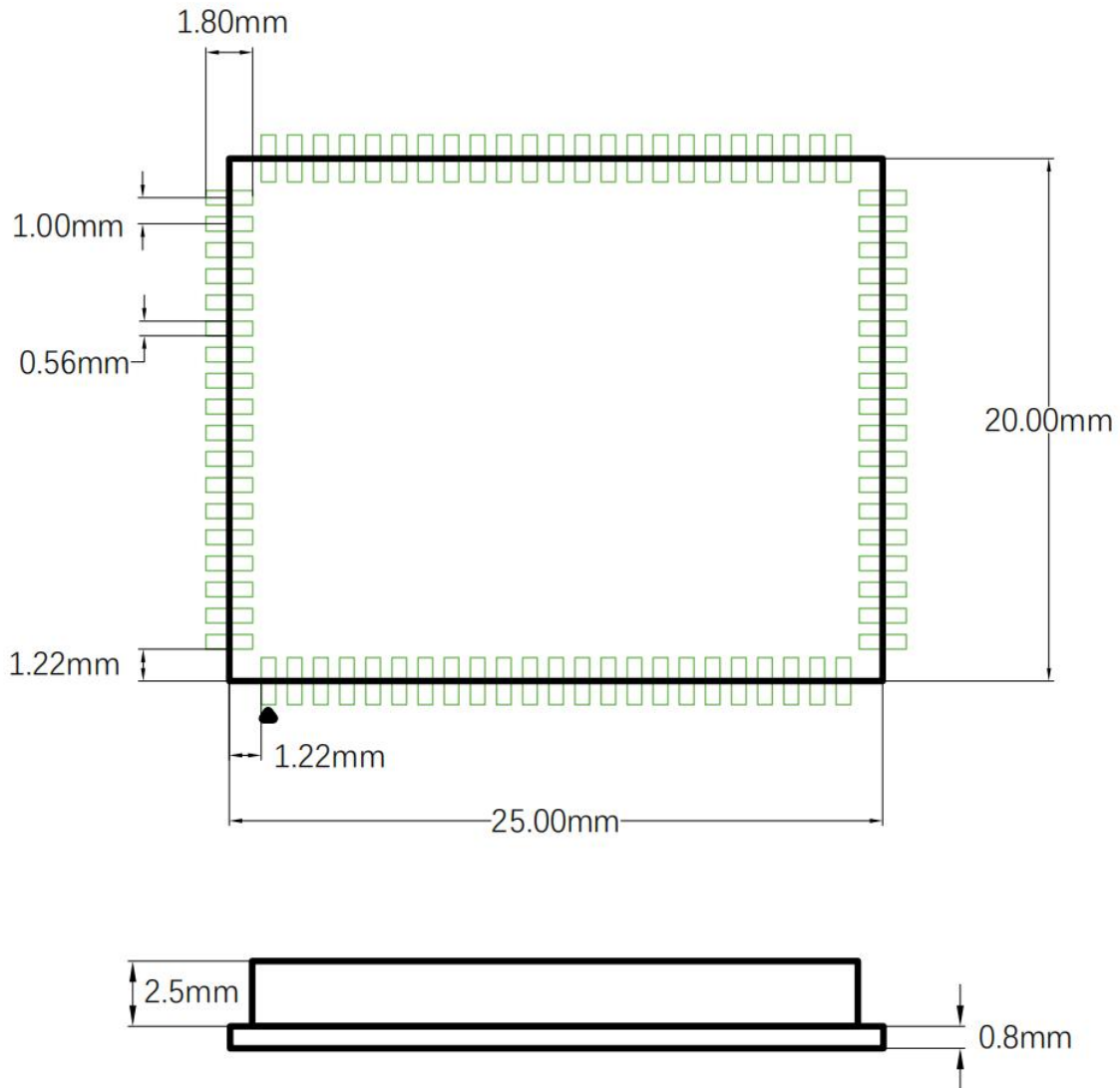


Figure 9: Dimension figure of WT0132P4-A1

7. Storage Condition

| Prerequisite | Parameters |
|----------------------|---|
| Storage condition | Non-condensing atmosphere < 40°C /90 %RH in sealed MBBs |
| Conditions of use | 168 hours at 25 ± 5°C , 60 % RH. |
| Moisture sensitivity | 3 levels |

8. Reflow Soldering Curve

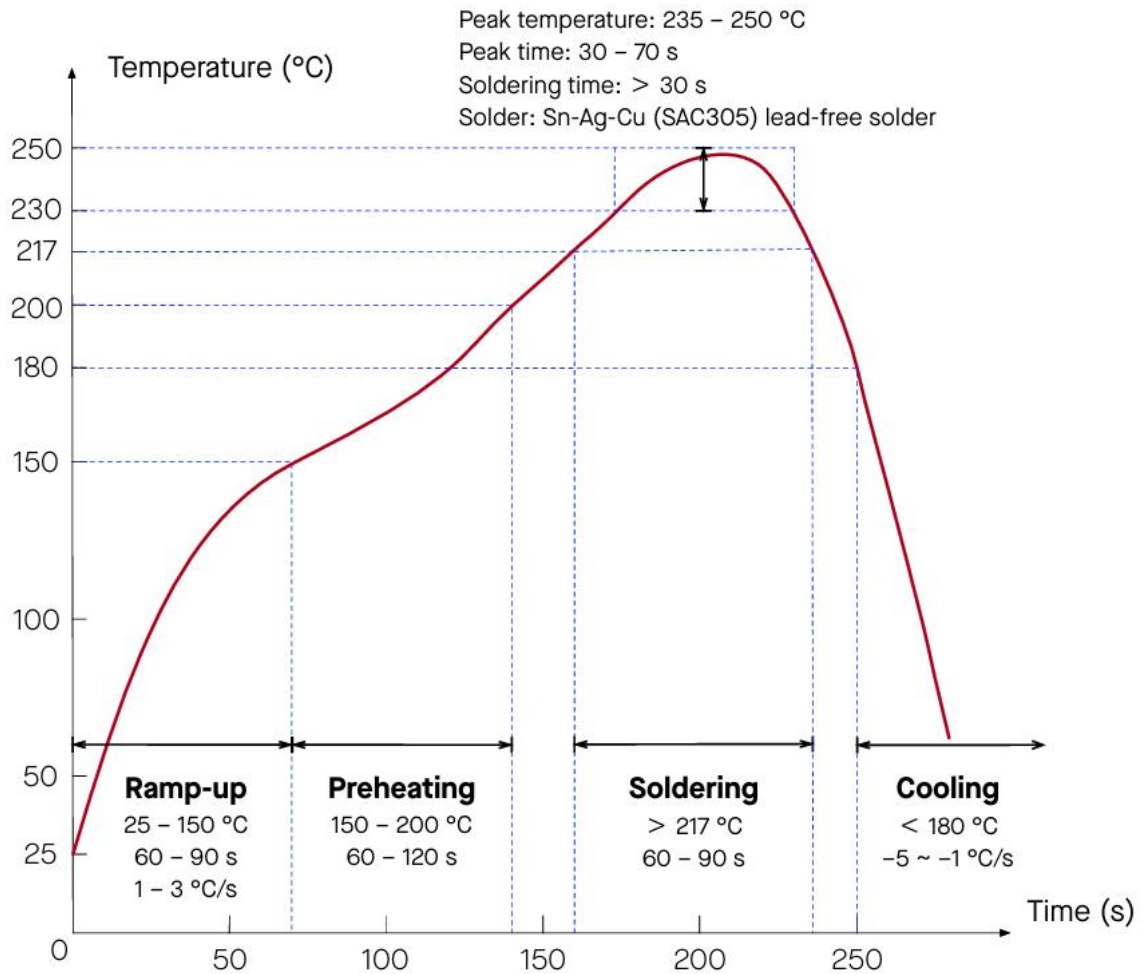


Figure 10: Reflow Soldering Temperature Curve

9. Contact Us

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