



恒芯微电子
HCT MICRO

HCT8X18 数据手册

删减版

| | |
|----------|-----|
| Version: | 1.0 |
|----------|-----|

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概述

HCT8X18 为 SPI 接口的 8 独立通道、16BIT 高精度 DAC 芯片。内置 2.5V 5ppm/°C 的基准电压源，具有 1/2、1、2 倍的放大倍数，对应 1.25V、2.5V、5V 的满量程输出信号。

主要指标

- 工作电压范围：2.7~5.5V
- 8 通道 16 位精度 DAC
 - DNL: 1LSB Typ
 - INL: 2.5LSB Typ
 - TUE: 0.1% Max
 - 动态特性：输出 1kHz 正弦波时，SFDR>80dB
- 内置 2.5V 基准电压源
 - 温度系数：5ppm/°C Typ
 - 初始精度：0.05% Max
 - 可配置为使用外部输入的基准电压
- 高驱动能力：+/-10mA
- 灵活的配置：
 - 增益：1/2、1、2 倍
 - 复位为零码值或中码值
- SPI 接口
 - 支持标准 4 线 SPI 8 bit 接口
 - 支持最高 50M 通信时钟
 - 支持写入读取 CRC 校验保护
- 工作电流：
 - 工作模式：3.1mA@8 通道全输出
0.33mA 每通道
 - 休眠模式：3.1uA
- 封装样式：
 - HCT8118: TSSOP16
 - HCT8018: WQFN16
- 工作温度范围：-40~+125°C

1. 性能指标

1.1. 极限参数

当外部输入或是环境参数超过下面条件时，很可能对芯片造成损坏或是缩短其使用寿命。下表只代表会造成损坏的范围，不代表可以正常工作的范围。

表 1-1 极限参数表

| 名称 | 参数 | 最小值 | 最大值 | 单位 |
|----------|------|------|------|----|
| VDD-AVSS | 电源电压 | -0.3 | +6 | V |
| TS | 存储温度 | -50 | +150 | °C |
| TJ | 工作温度 | -40 | +125 | °C |

1.2. 工作参数

表 1-2 工作参数表

| 名称 | 参数 | 最小值 | 典型值 | 最大值 | 单位 |
|--------|--------------------------|-----|-----|---------------|----|
| VDD | 模拟电源电压 | 2.7 | 5 | 5.5 | V |
| VIO | 数字 IO 电源 | 1.7 | | 5.5 | |
| VPOR | 上电复位电压 | 1.9 | 2 | 2.1 | V |
| VLVD | 掉电监测电压 | 2.8 | 2.9 | 3 | V |
| TA | 温度范围 | -40 | 25 | 125 | °C |
| VREFIN | VDD 2.7~3.3V, REFDIV=0 时 | 1.2 | | (VDD - 0.2)/2 | V |
| | VDD 2.7~3.3V, REFDIV=1 时 | 2.4 | | VDD - 0.2 | V |
| | VDD 3.3~5.5V, REFDIV=0 时 | 1.2 | | VDD/2 | V |

| | | | | | |
|--|--------------------------|-----|--|-----|---|
| | VDD 3.3~5.5V, REFDIV=1 时 | 2.4 | | VDD | V |
|--|--------------------------|-----|--|-----|---|

1.3. ESD/LU 性能

表 1-3 ESD/Latch-Up 性能指标

| 名称 | 参数 | 最小值 | 最大值 | 单位 |
|----------|-----------------------|-------|------|----|
| ESD(HBM) | HBM 模型的 ESD 放电电压 | -4000 | 4000 | V |
| Latch-Up | Latch-Up 测试电流 (@85°C) | -200 | 200 | mA |

1.4. GPIO 参数

表 1-5 GPIO 参数表

| 名称 | 参数 | VIO | 最小值 | 典型值 | 最大值 | 单位 |
|-----|-------------------|-----|------|------|------|----|
| VIH | 输入信号高阈值 | 5V | 4 | | 5.5 | V |
| VIL | 输入信号低阈值 | 5V | -0.3 | | 1 | V |
| VT+ | 施密特由低变高电压的阈值 | 5V | 2.72 | 2.92 | 3.17 | V |
| VT- | 施密特由高变低电压的阈值 | 5V | 3.15 | 2 | 2.17 | V |
| IIH | 输入高电平的电流 | 5V | | | +1 | uA |
| IIL | 输入低电平的电流 | 5V | -1 | | | uA |
| VOL | 输出低电平 (@IOL 电流条件) | 5V | | | 0.4 | V |
| VOH | 输出高电平 (@IOH 电流条件) | 5V | 4 | | | V |
| IOL | 输出低电平电流@VOL (max) | 5V | 4.9 | 8.8 | 13.9 | mA |
| IOH | 输出高电平电流@VOH (min) | 5V | 5.5 | 15.6 | 29.9 | mA |

1.5. 模拟性能参数

表 1-8 模拟性能参数表

| 参数 | 测试条件 | 最小值 | 典型值 | 最大值 | 单位 |
|------------------------|--|-----|---------|----------|---------------|
| 静态参数 | | | | | |
| Resolution | | 16 | | | Bits |
| INL | TA = 25°C | | +/-2.5 | +/-5 | LSB |
| DNL | TA = 25°C | | +/-1 | +/-2 | LSB |
| TUE | TA = 25°C | | +/-0.05 | +/-0.12 | %FSR |
| Offset error | | 0 | 0.8 | 1.6 | mV |
| Zero-code error | DAC code = zero scale | | 0.5 | 1 | mV |
| Full-scale error | | | +/-0.05 | +/-0.1 | %FSR |
| Gain error | | | +/-0.05 | +/-0.1 | %FSR |
| Offset error drift | | | 2 | | μV/°C |
| Zero-code error drift | | | 2 | | μV/°C |
| Full-scale error drift | | | 2 | | ppm of FSR/°C |
| Gain error drift | | | 2 | | ppm of FSR/°C |
| Voltage range | Gain = 2 (BUFFGAIN = 1, REFDIV = 0) | 0 | | 2 * VREF | V |
| | Gain = 1 (BUFFGAIN = 0, REFDIV = 0 或 BUFFGAIN = 1, REFDIV = 1) | 0 | | VREF | V |

| | | | | | |
|------------------------------|--|-------|------|--------|-------|
| | Gain = 1/2 (BUFFGAIN = 0, REFDIV = 1) | 0 | | VREF/2 | V |
| Output voltage headroom | to GND or VDD (unloaded) | 0.002 | | | V |
| | to GND or VDD (-5 mA ≤ IOUT ≤ 5 mA) | 0.2 | | | V |
| | to GND or VDD (-10 mA ≤ IOUT ≤ 10 mA) | 0.4 | | | V |
| Short circuit current | DAC code = full scale. Output shorted to GND | | 26 | | mA |
| | DAC code = zero scale. Output shorted to VDD | | 26 | | mA |
| Load regulation | DAC code = midscale -10 mA ≤ IOUT ≤ 10 mA | | 150 | | μV/mA |
| Maximum capacitive load | RLOAD = ∞ | 0 | | 2 | nF |
| | RLOAD = 2 kΩ | 0 | | 10 | nF |
| DC output impedance | DAC code = midscale | | 0.15 | | Ω |
| | DAC output at GND or VDD | | 25 | | Ω |
| 动态参数 | | | | | |
| Output voltage settling time | ¼ to ¾ scale and ¾ to ¼ scale settling time to ±2 LSB, VDD = 5.5 V, VREFIN = 2.5 V, Gain = 2, CLoad=2nF | | 3 | | μs |
| Slew rate | VDD = 5.5 V, VREFIN = 2.5 | | 1.4 | | V/μs |

| | | | | | |
|----------------------------------|--|--|-----|--|--------|
| | V, Gain = 2, CLoad=2nF | | | | |
| SFDR | VDD = 5.5 V, VREFIN = 2.5 V, Gain = 2 | | 80 | | dB |
| Power-up time | DACx-PWDWN 1 to 0 transition. DAC code = full scale. VDD = 5.5 V, VREFIN = 2.5 V, Gain = 2 | | 5 | | μs |
| Power-up glitch magnitude | DAC code = zero scale. VDD = 5.5 V, VREFIN = 2.5 V, Gain = 2. CLOAD = 50 pF | | 30 | | mV |
| Output noise | 0.1 Hz to 10 Hz, DAC code = midscale, VDD = 5.5 V, VREFIN = 2.5 V, Gain = 2 | | 16 | | μVpp |
| Output noise density | 1 kHz, DAC code = midscale, VDD = 5.5 V, VREFIN = 2.5 V, Gain = 2 | | 120 | | nV/√Hz |
| | 10 kHz, DAC code = midscale, VDD = 5.5 V, VREFIN = 2.5 V, Gain = 2 | | 115 | | nV/√Hz |
| | 1 kHz, DAC code = full scale, VDD = 5.5 V, VREFIN = 2.5 V, Gain = 1 | | 85 | | nV/√Hz |
| | 10 kHz, DAC code = full scale, VDD = 5.5 V, VREFIN = 2.5 V, Gain = 1 | | 78 | | nV/√Hz |
| AC PSRR | DAC code = midscale, | | 87 | | dB |

| | | | | | |
|--|--|--------|-----|--------|--------|
| | frequency = 60 Hz | | | | |
| Code change glitch impulse | 1 LSB change | | 2 | | nV-s |
| Channel to Channel AC crosstalk | DAC code = midscale. Code 32 to full-scale swing on adjacent channel | | 0.2 | | nV-s |
| 外部输入基准电压源 | | | | | |
| Reference input current | VREFIN = 2.5 V | | 21 | | μA |
| Reference input impedance | | | 120 | | kΩ |
| Reference input capacitance | | | 5 | | pF |
| 内部基准电压源 | | | | | |
| Reference output voltage | TA = 25°C | 2.4975 | 2.5 | 2.5025 | V |
| Reference output drift | | | 4 | 10 | ppm/°C |
| Reference output impedance | | | 0.1 | | Ω |
| Reference output noise | 0.1 Hz to 10 Hz | | 16 | | μVpp |
| Reference output noise density | 10 kHz, REFLOAD = 10 nF | | 180 | | nV/√Hz |
| Reference load current | | | ±10 | | mA |
| Reference load regulation | Source and sink | | 80 | | μV/mA |

| | | | | | |
|----------------------------------|---|--|------|--|------------------------|
| Reference line regulation | | | 20 | | $\mu\text{V}/\text{V}$ |
| Reference output drift over time | TA = 25°C, 1000 hours | | 50 | | ppm |
| Reference thermal hysteresis | First cycle | | 100 | | ppm |
| | Additional cycle | | 30 | | |
| 功耗 | | | | | |
| VDD supply current | Active mode. Internal reference enabled. Gain = 1. DAC code = full scale. Outputs unloaded. SPI static | | 3.23 | | mA |
| | Active mode. Internal reference disabled. Gain = 1. DAC code = full scale. Outputs unloaded. SPI static | | 3.1 | | mA |
| | Power-down | | 1.8 | | μA |
| VIO supply current | | | 2 | | μA |

1.6. 测试数据

测试条件:

如无特殊说明, AVDD=5V, 25 摄氏度, 无输出滤波电容, 使用内部 2.5V 基准电压, GAIN=1。

部分测试波形为交流耦合方式抓取, 目的是看基准电压随负载或电源跳变的波动幅度和稳定时间。

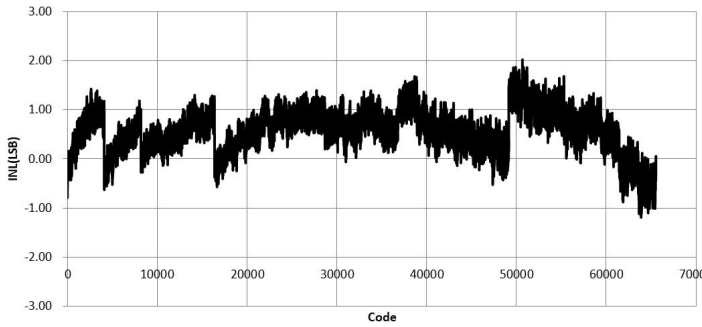


Figure 1-1 INL Vs Code

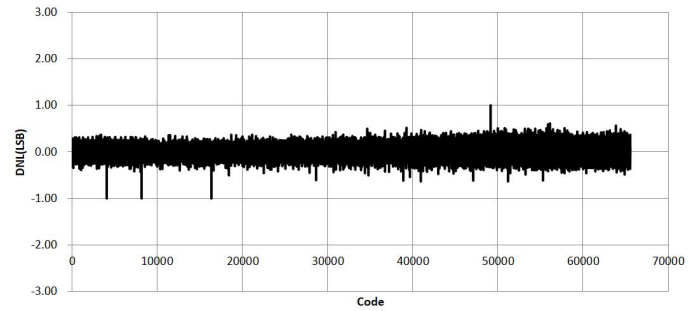


Figure 1-2 DNL Vs Code

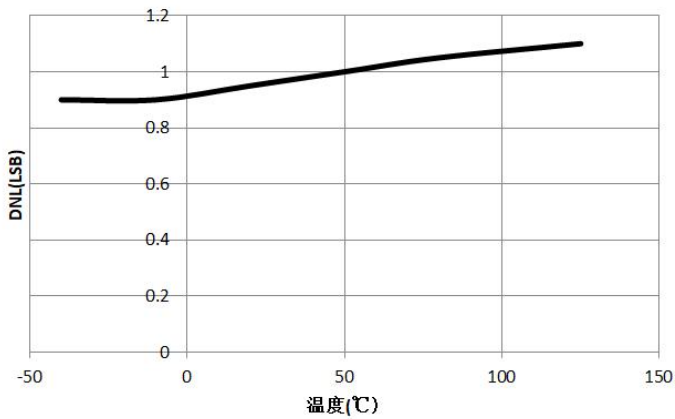


Figure 1-3 DNL Vs Temp

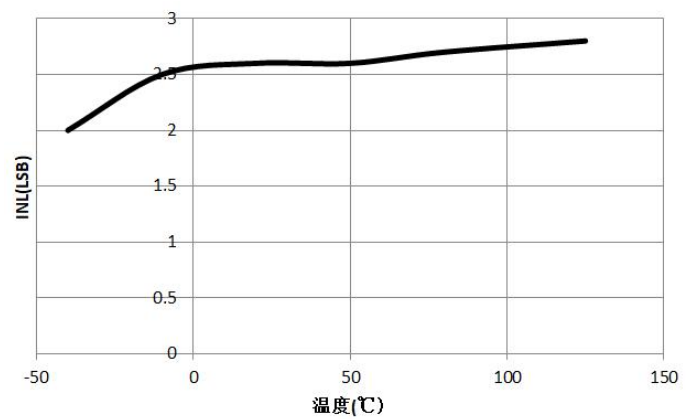


Figure 1-4 INL Vs Temp

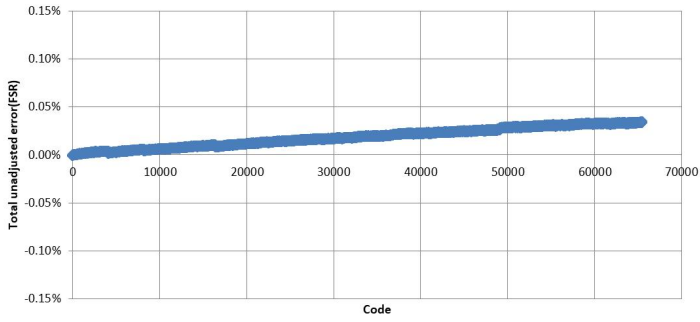


Figure 1-5 TUE Vs Code

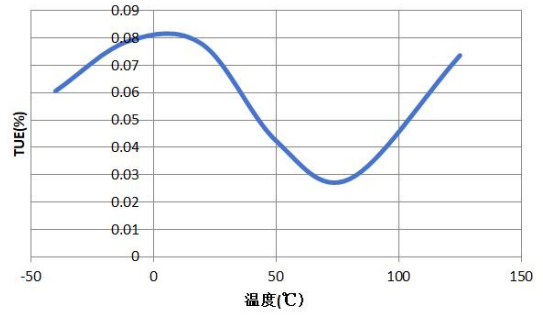


Figure 1-6 TUE Vs Temp

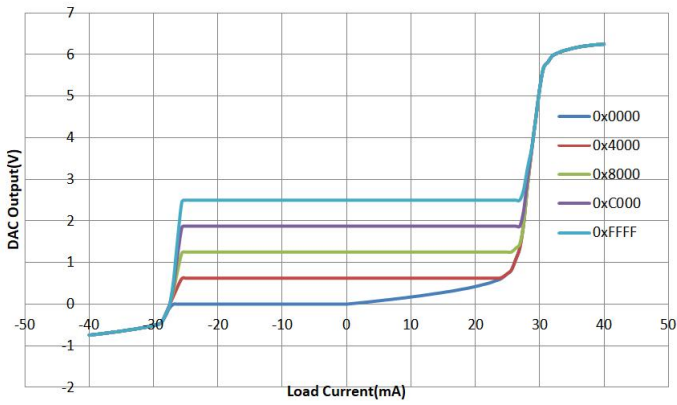


Figure 1-7 Source and Sink Capability with G=1

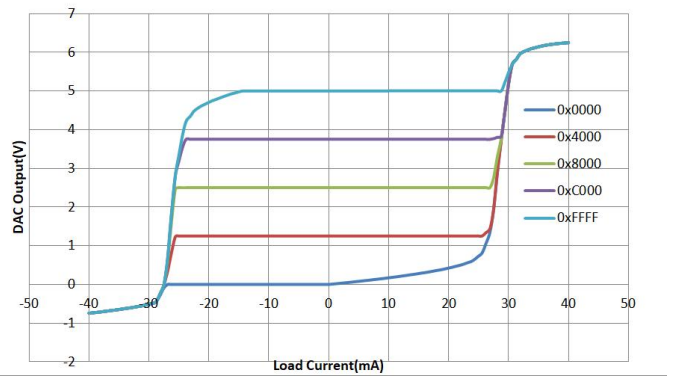


Figure 1-8 Source and Sink Capability with G=2

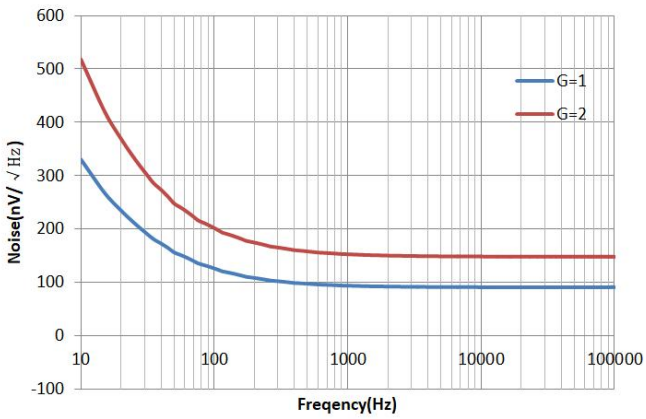


Figure 1-9 Noise density VS Frequency

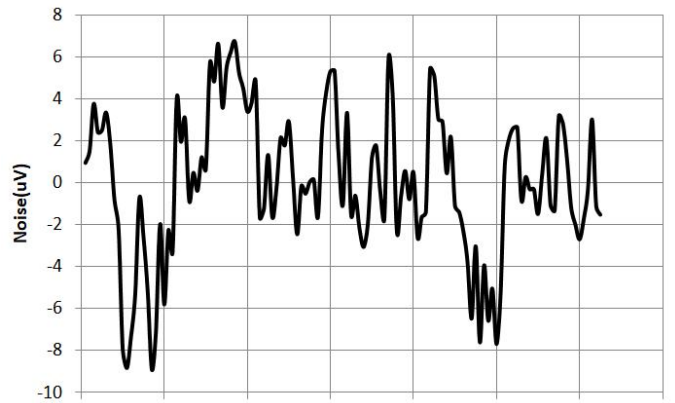


Figure 1-10 Output noise with internal VREF 0.1Hz~10Hz

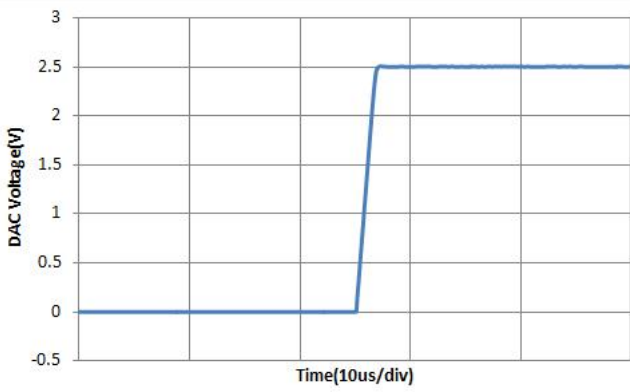


Figure 1-11 Full scale settling time, Rising edge

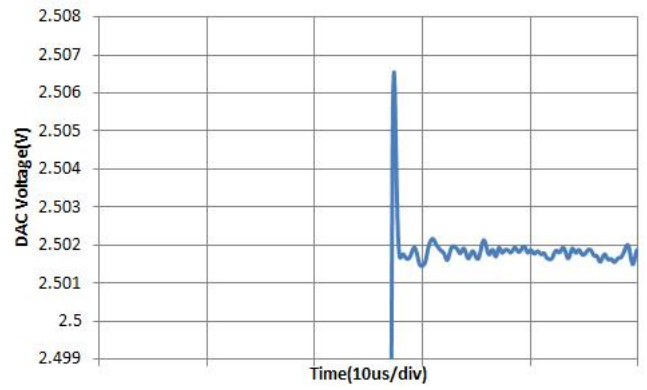


Figure 1-12 Full scale settling time, Rising edge, small signal

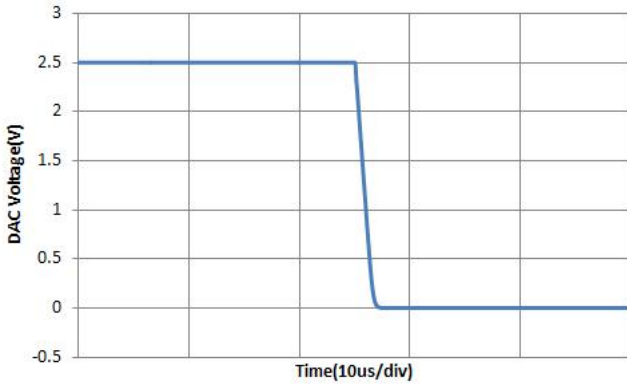


Figure 1-13 Full scale settling time, Falling edge

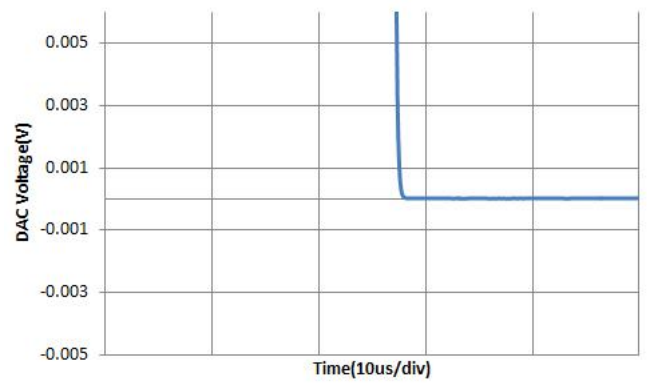


Figure 1-14 Full scale settling time, Falling edge, small signal

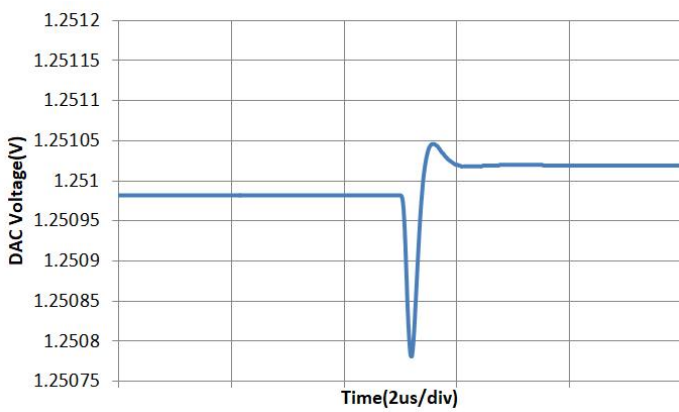


Figure 1-15 1LSB step settling time, Rising edge

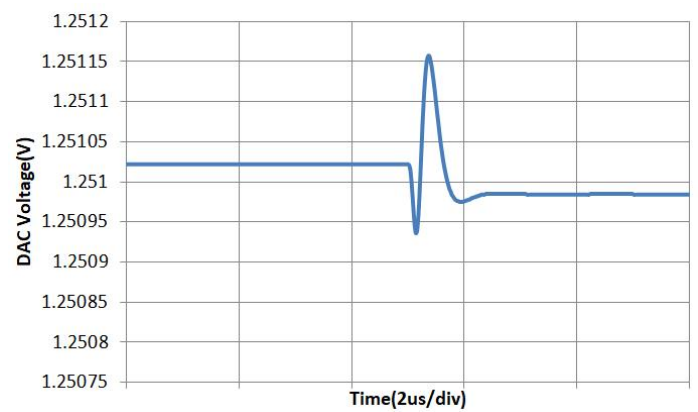


Figure 1-16 1LSB step settling time, Falling edge

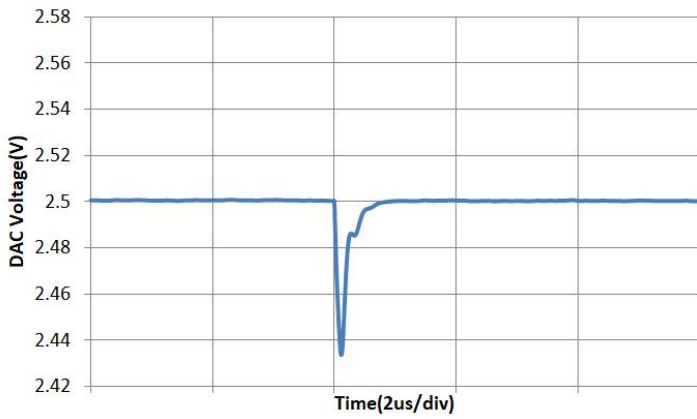


Figure 1-17 Load Current change from -1mA to 1mA

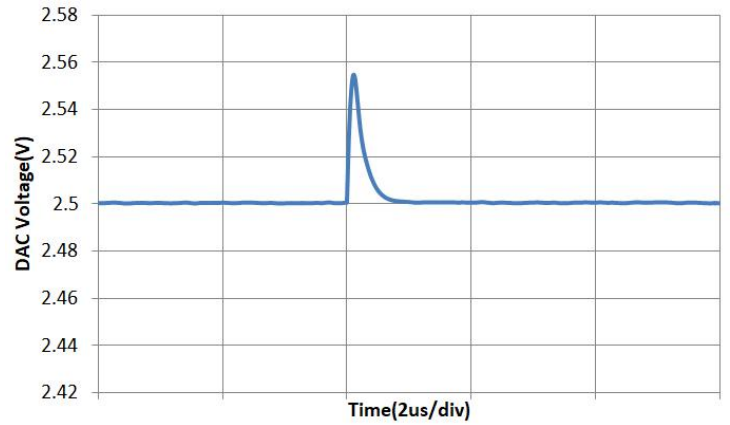


Figure 1-18 Load Current change from -1mA to 1mA

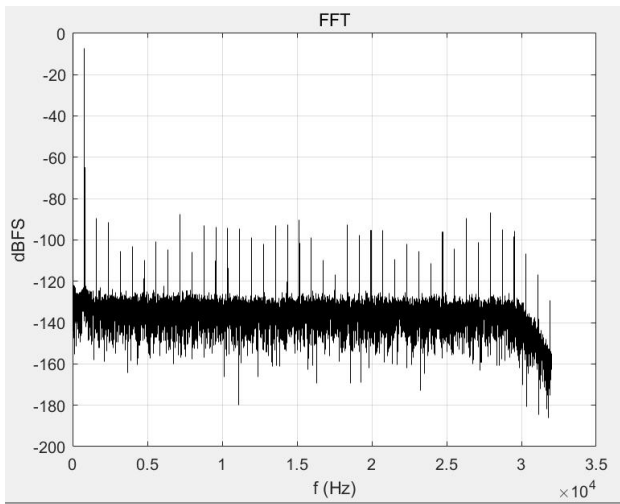


Figure 1-19 1kHz Sine wave output spectrum, 64kHz sampling rate

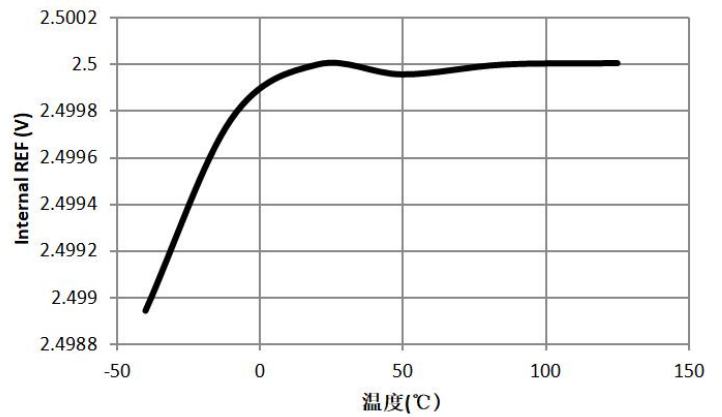


Figure 1-20 Internal reference VS temp

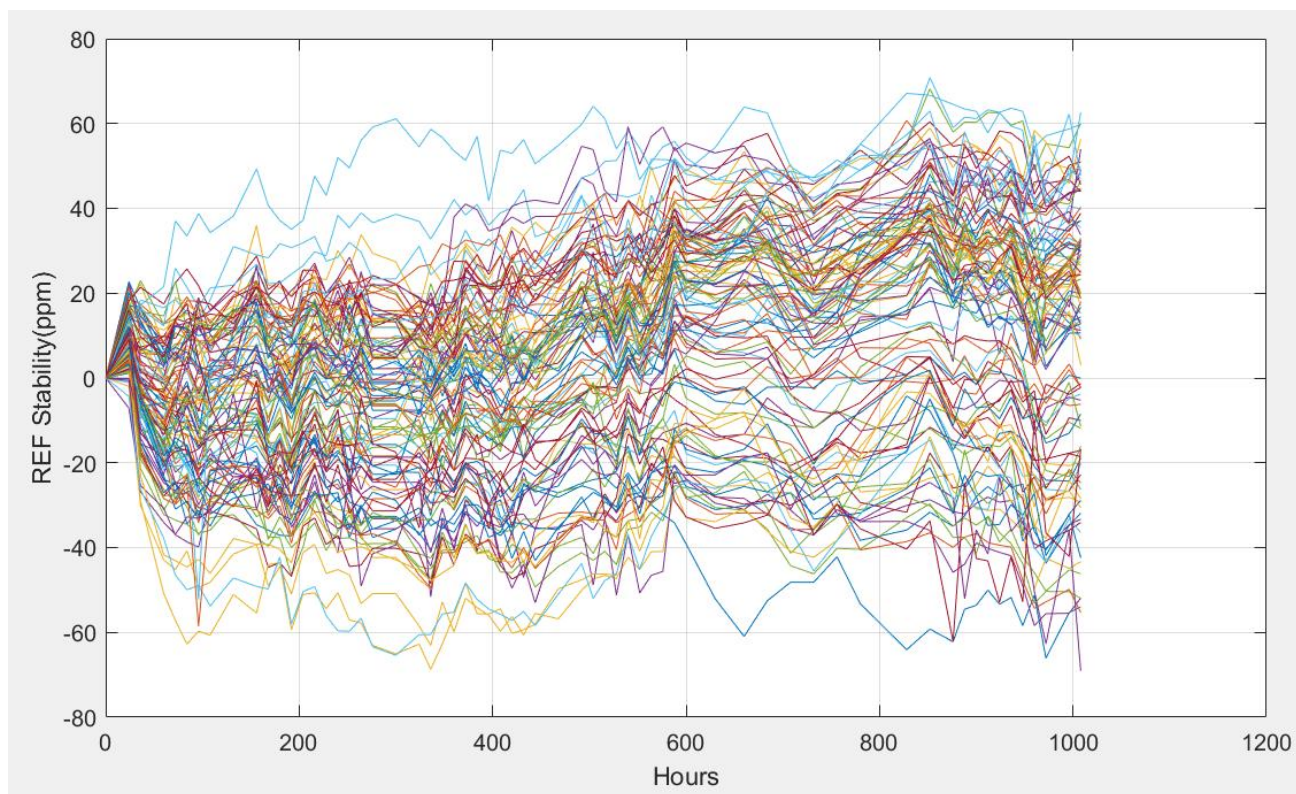


Figure 1-21 Internal Reference Long-Term stability(1000 Hours, 100 samples)

2. 引脚定义和封装

2.1. 引脚定义

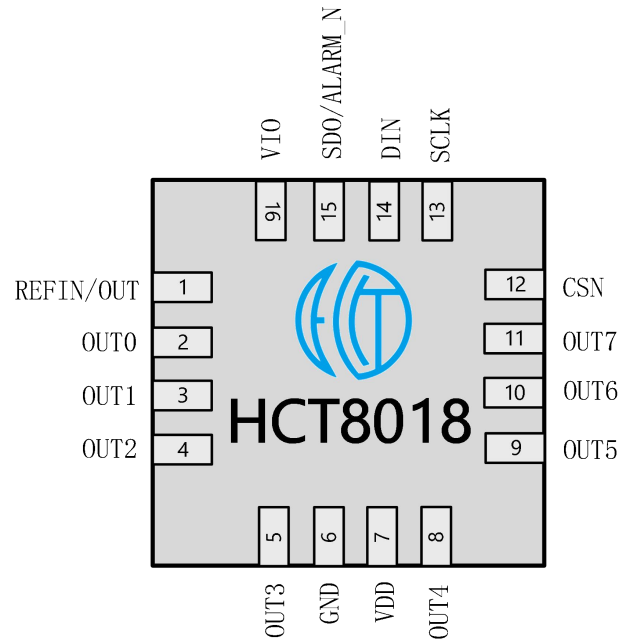


Figure 2-1 HCT8018 芯片引脚图

Table 2-1 HCT8018 引脚定义

| 引脚 | 名称 | 类型 | 描述 |
|----|--------------|-------|----------|
| 1 | REFIN/REFOUT | 输入/输出 | 基准源输入/输出 |
| 2 | OUT0 | 输出 | DAC0 输出 |
| 3 | OUT1 | 输出 | DAC1 输出 |
| 4 | OUT2 | 输出 | DAC2 输出 |
| 5 | OUT3 | 输出 | DAC3 输出 |
| 6 | GND | 地 | 芯片地 |
| 7 | VDD | 电源 | 模拟部分电源 |
| 8 | OUT4 | 输出 | DAC4 输出 |
| 9 | OUT5 | 输出 | DAC5 输出 |
| 10 | OUT6 | 输出 | DAC6 输出 |
| 11 | OUT7 | 输出 | DAC7 输出 |

| | | | |
|----|-----------|----|----------------------------|
| 12 | CSN | 输入 | SPI 片选输入，低电平有效 |
| 13 | SCLK | 输入 | SPI 时钟输入 |
| 14 | DIN | 输入 | SPI 数据输入 |
| 15 | SDO/ALARM | 输出 | SPI 数据输出，片外需有 10 Kohm 上拉电阻 |
| 16 | VIO | 电源 | 数字接口部分电源 |

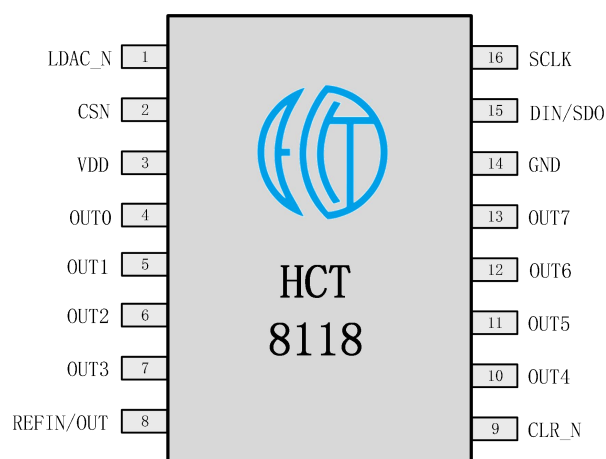
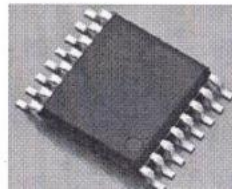
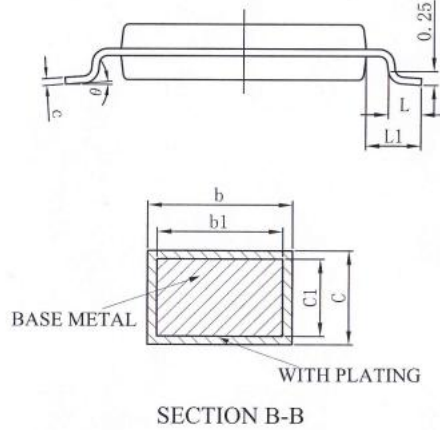
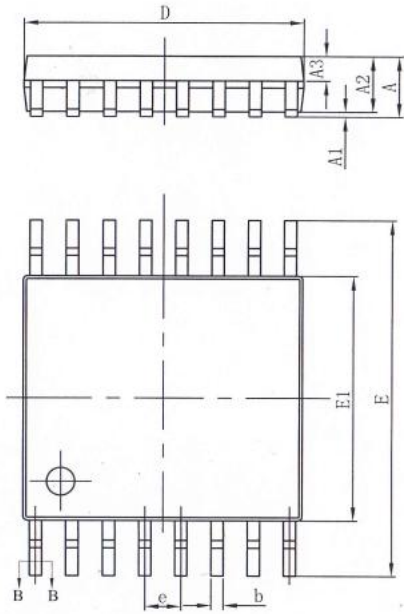


Figure 2-1 HCT8118 芯片引脚图

| 引脚 | 名称 | 类型 | 描述 |
|----|--------------|-------|---|
| 1 | LDAC_N | 输入 | DAC 数据锁存控制，当此信号由 1 => 0，所有设为 sync mode 的 DAC 通道数据会更新到输出 |
| 2 | CSN | 输入 | SPI 片选输入，低电平有效 |
| 3 | VDD | 电源 | 芯片电源 |
| 4 | OUT0 | 输出 | DAC0 输出 |
| 5 | OUT1 | 输出 | DAC1 输出 |
| 6 | OUT2 | 输出 | DAC2 输出 |
| 7 | OUT3 | 输出 | DAC3 输出 |
| 8 | REFIN/REFOUT | 输入/输出 | 基准源输入/输出，外接 1uF 滤波电容 |
| 9 | CLR_N | 输入 | DAC 数据复位控制，当此信号由 0 => 1，DAC 数据将会复位 |
| 10 | OUT4 | 输出 | DAC4 输出 |
| 11 | OUT5 | 输出 | DAC5 输出 |
| 12 | OUT6 | 输出 | DAC6 输出 |
| 13 | OUT7 | 输出 | DAC7 输出 |
| 14 | GND | 地 | 芯片地 |
| 15 | DIN/SDO | 输入 | SPI 数据输入/输出 |
| 16 | SCLK | 输入 | SPI 时钟输入 |

2.2. 封装尺寸

HCT8118: TSSOP16



| SYMBOL | MILLIMETER | | |
|--------|------------|------|------|
| | MIN | NOM | MAX |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.90 | 1.00 | 1.05 |
| A3 | 0.39 | 0.44 | 0.49 |
| b | 0.20 | — | 0.28 |
| b1 | 0.19 | 0.22 | 0.25 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 4.90 | 5.00 | 5.10 |
| E | 6.20 | 6.40 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | 0.65BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00BSC | | |
| θ | 0 | — | 8° |