

深圳触觉智能科技有限公司
产 品 规 格 书

7寸1024*600 MIPI屏幕/1050010036
配100mm排线/1050040017

Project No. 项目编号	F700035	
Customer 客户名称		
Module No. 客户型号		
Product type 产品内容	Standard LCD Module 1024x 3RGB x 600 Dots 7.0" TFT LCD	
Signature by customer: 客户确认签章:		
PREPARED BY	CHECKED BY	APPROVED BY

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1 Document revision history :

DOCUMENT REVISION	DATE	DESCRIPTION	PREPARED BY	APPROVED BY
A	2022.07.28	First Release.	XIANG	

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2. General Feature:

Item	Standard Value	Unit
Display Size	7.0"	--
Number of Pixels	1024(H)x3(RGB)x600(V)	--
Active Area	154.2144(L) *85.92(W)	mm
Pixel pitch	0.1506(L) × 0.1432(W)	mm
Outline Dimension	165(L) ×100(W) × 4.95(T)	mm
Pixel Arrangement	RGB island	-
Display Mode	Normally Black	-
Number of color	16.7M	-
Viewing Direction	ALL	-
Interface	MIPI interface	-
Driver IC	EK79007+EK73217	-
Driver Condition	3.3V	V
Backlight	White LED	-
Touch Panel	Touch Panel	-
Operation Temperature	-10~60	℃
Storage Temperature	-20~70	℃

[illegible]

4.Pin Description

Pin NO.	Symbol	Description
1~2	LEDA	Backlight LED Anode
3	LCD_VGH	Positive power output of the VGH step up circuit
4	LCD_VGL	Negative power output of the VGL step up circuit
5	UPDN	Gate up or down scan control
6	SHLR	Source right or left sequence control
7~8	LEDK	Backlight LED Cathod
9	LCD_10V	Voltage regulator output for logic circuit(+10V)
10	GND	Ground
11	D3P	DSI Data differential signal input pins. (Data lane3)
12	D3N	DSI Data differential signal input pins. (Data lane3)
13	GND	Ground
14	D2P	DSI Data differential signal input pins. (Data lane2)
15	D2N	DSI Data differential signal input pins. (Data lane2)
16	GND	Ground
17	CLKP	DSI CLOCK differential signal input pi
18	CLKN	DSI CLOCK differential signal input pi
19	GND	Ground
20	D1P	DSI Data differential signal input pins. (Data lane1)
21	D1N	DSI Data differential signal input pins. (Data lane1)
22	GND	Ground
23	D0P	DSI Data differential signal input pins. (Data lane0)
24	D0N	DSI Data differential signal input pins. (Data lane0)
25	GND	Ground
26	STBYB	Standby mode, normally pull high
27	LRSTB	Reset Signal pin (“Low” is enabl)
28	VDD	Power supply(3.3V)
29	VDD	Power supply(3.3V)
30	VCOM	Common voltage

5. Electrical Characteristics

5-1 TFT LCD Module Operating Conditions

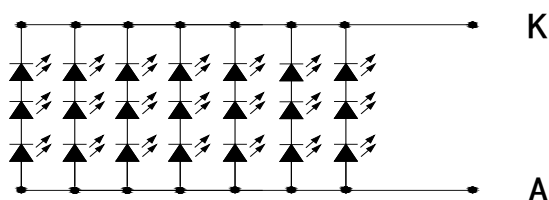
Item	Symbol	Min	Type	Max	Unit
Digital Voltage	DVDD	1.8	3.3	3.5	V
Analog Voltage	AVDD	9.4	9.6	9.8	V
Gate Driver High Voltage	VGH	17	18	19	V
Gate Driver Low Voltage	VGL	-6.5	-6.0	-5.5	V
Input signal voltage	VCOM	3.2	(3.6)	4.0	V
Input logic high voltage	VIH	0.7DVDD	-	DVDD	V
Input logic low voltage	VIL	GND	-	0.3DVDD	V
Output logic high voltage	VOH	DVDD-0.4	-	DVDD	V
Output logic low voltage	VOL	GND	-	GND+0.4	V

5-2 LED back light specification (per a chip)

Item	Symbol	Min	Type	Max	Unit
Forward voltage	V_F	-	21	-	V
Forward current	I_F	-	140	-	mA
Luminance	L_v	-	250	-	cd/m ²
Power Consumption	P_{LED}	-	2940	-	mW
Uniformity(with L/G)	Avg	75	80	-	%
LED Life-Time	Hr	-	30000	-	Hour

Note 1: The LED Supply Voltage is defined by the number of LED at $T_a=25^{\circ}\text{C}$ and $I_L=20\text{mA/LED}$.

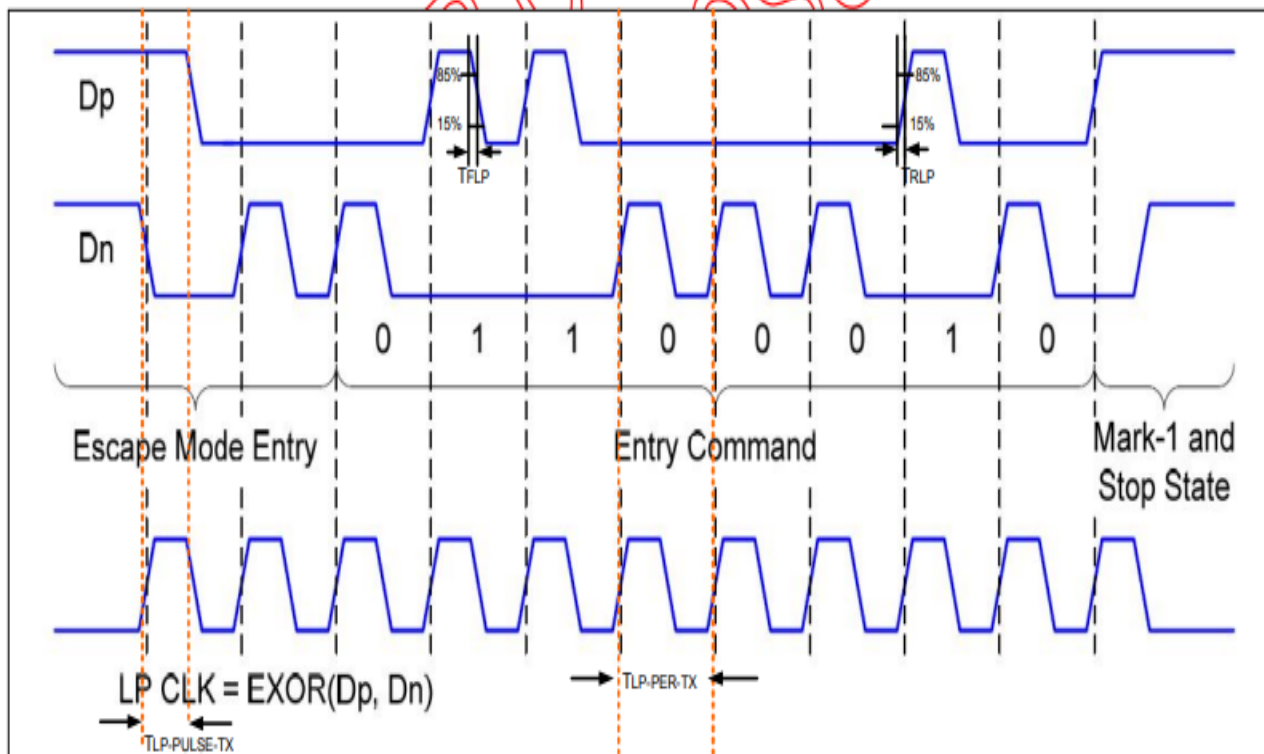
Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at $T_a=25^{\circ}\text{C}$ and $I_L=20\text{mA/LED}$. The LED lifetime could be decreased if operating I_L is large than 20mA/LED.



6. Timing Characteristics of Input Signals

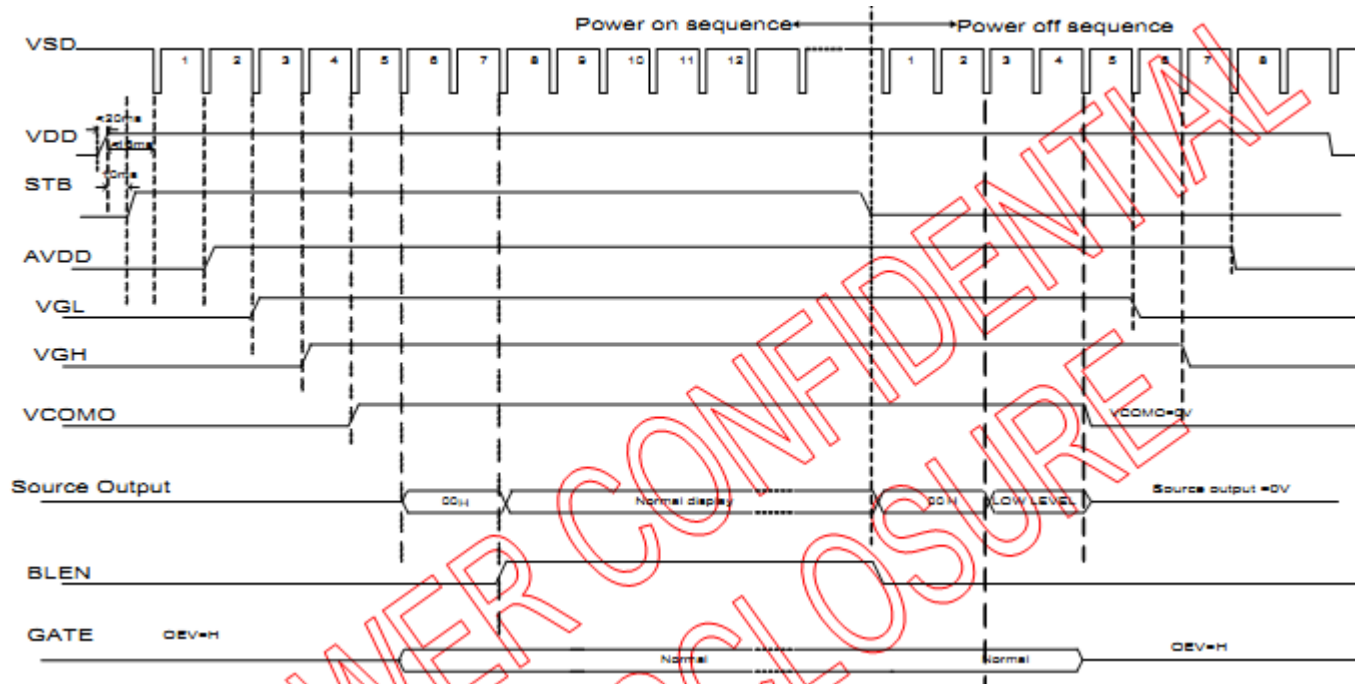
6-1 Data Input Format

Parameter	Symbol	Min	Typ	Max	Units	Notes
15%~85% rising time and falling time	T_{RLP} / T_{FLP}	-	-	25	ns	-
30%~85% rising time and falling time	T_{REOT}	-	-	35	ns	-
Pulse width of LP exclusive-OR clock	First LP EXOR clock pulse after STOP state or Last pulse before stop state	$T_{LP-PULSE-TX}$	40	-	-	ns
All other pulses		20	-	-	-	ns
Period of the LP EXOR clock	$T_{LP-PER-TX}$	90	-	-	mV/ns	-
Slew Rate @CLOAD =0pF	$\delta V / \delta t_{SR}$	30	-	500	mV/ns	-
Slew Rate @CLOAD =5pF		30	-	200	mV/ns	-
Slew Rate @CLOAD =20pF		30	-	150	mV/ns	-
Slew Rate @CLOAD =70pF		30	-	100	mV/ns	-
Load Capacitance	T_{RLP}	-	-	70	pF	-

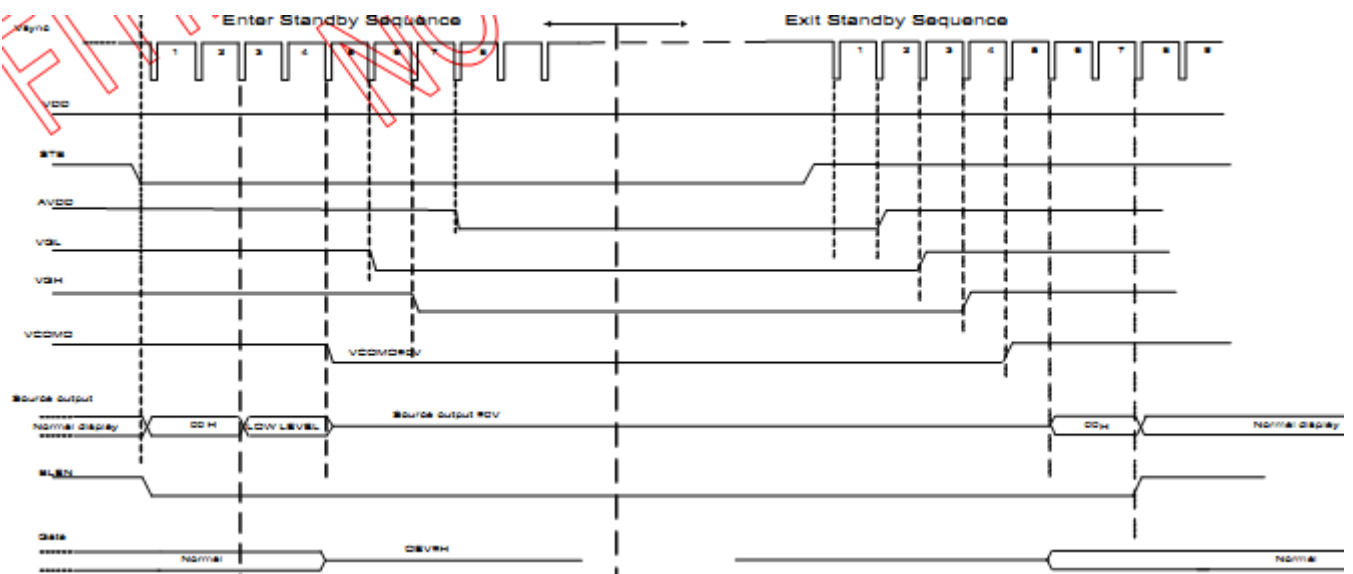


7.Power Function Description

7-1 Power On/Off Sequence



7-2 Enter and Exit Standby Mode Sequence



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8. Optical Characteristics

Item	Symbol	Condition	Min	Type	Max	Unit
Transmittance(w/o DBEF)	T%		4.8	5.0	-	%
Contrast Ratio	CR		-	800	-	-
Response time	tr+tf		-	30	40	ms
Viewing Angle	Top	$CR \geq 10$	80	85	-	Deg.
	Bottom		80	85		
	Left		80	85		
	Right		80	85		
Color of CIE Coordinate	W	x	-	0.308	-	
		y	-	0.336	-	
	R	x	-	0.599	-	
		y	-	0.338	-	
	G	x	-	0.299	-	
		y	-	0.550	-	
	B	x	-	0.139	-	
		y	-	0.131	-	

9. RELIABILITY TEST

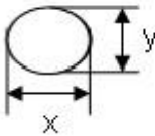
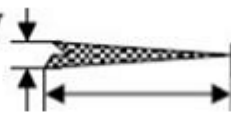
No	Test items	Conditions	Remark
1	High Temp.Storage	Ta=+70°C,48hrs	
2	Low Temp. Storage	Ta=-20°C,48hrs	
3	High Temp.Operation	Ta=+60°C,48hrs	
4	Low Temp. Operation	Ta=-10°C,48hrs	
5	High Temp./Humi. Storage	Ta=+60°C,90%RH,48hrs	
6	Thermal Shock	-10°C /30min← →+60°C/30min, Change time:5min,10cycles	

10. Incoming Inspection Standards

10- 1 Major defect

No.	Item	Inspection Standard	Classification of defects
1	All functional defects	1) No display 2) Display abnormally 3) Open or missing segment 4) Short circuit 5) Excess power consumption 6) Backlight no lighting, flickering and abnormal lighting	Major
2	Missing	Missing component	Major
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	Major

10- 2 Cosmetic Defect

No.	Item	Inspection Standard		Classification of defects										
1	(spot defect) Black and White spot pinhole	For dark/white spot, size Φ is defined as $\Phi=(x+y)/2$		Minor										
		<table><tr><th>Size Φ (mm)</th><th>Acceptable Quantity</th></tr><tr><td>$\Phi \leq 0.1$</td><td>Ignore</td></tr><tr><td>$0.10 \leq \Phi \leq 0.15$</td><td>2</td></tr><tr><td>$0.15 \leq \Phi \leq 0.2$</td><td>1</td></tr><tr><td>$0.2 < \Phi$</td><td>0</td></tr></table>			Size Φ (mm)	Acceptable Quantity	$\Phi \leq 0.1$	Ignore	$0.10 \leq \Phi \leq 0.15$	2	$0.15 \leq \Phi \leq 0.2$	1	$0.2 < \Phi$	0
		Size Φ (mm)	Acceptable Quantity											
		$\Phi \leq 0.1$	Ignore											
		$0.10 \leq \Phi \leq 0.15$	2											
$0.15 \leq \Phi \leq 0.2$	1													
$0.2 < \Phi$	0													
2	(line defect) Black and White line Polarizer scratch	Define: 	Minor											
		<table><tr><th>Width(mm)</th><th>Length(mm);Acceptable Qty</th></tr><tr><td>$\Phi \leq 0.03$</td><td>Ignore</td></tr><tr><td>$0.03 < W \leq 0.05$</td><td>$L \leq 3.0$; $N \leq 2$</td></tr><tr><td>$0.05 < W \leq 0.1$</td><td>$L \leq 2.0$; $N \leq 2$</td></tr><tr><td>$0.1 < W$</td><td>Define as spot defect</td></tr></table>		Width(mm)	Length(mm);Acceptable Qty	$\Phi \leq 0.03$	Ignore	$0.03 < W \leq 0.05$	$L \leq 3.0$; $N \leq 2$	$0.05 < W \leq 0.1$	$L \leq 2.0$; $N \leq 2$	$0.1 < W$	Define as spot defect	
		Width(mm)		Length(mm);Acceptable Qty										
		$\Phi \leq 0.03$		Ignore										
		$0.03 < W \leq 0.05$		$L \leq 3.0$; $N \leq 2$										
$0.05 < W \leq 0.1$	$L \leq 2.0$; $N \leq 2$													
$0.1 < W$	Define as spot defect													

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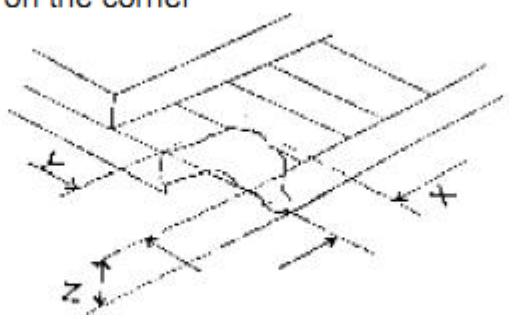
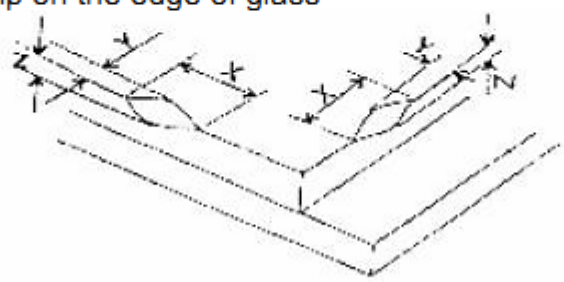
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3	Polarizer defect	Dent or bubble(between the polarizer and glass)		Minor
		Size Φ (mm)	Acceptable Qty	
		$\Phi \leq 0.10$	Ignor	
		$0.10 < \Phi \leq 0.20$	2	
		$0.20 < \Phi \leq 0.30$	1	
		$0.30 < \Phi$	0	

10- 3 Cosmetic Defect

No.	Item	Inspection Standard	Classification of defects						
1	Glass defect	1) Chip on the corner  <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0</td><td>≤S</td><td>≤T</td></tr></table> Remark: S=contact pad length; T=the thickness of glass Chips on the corner of terminal shall not be allowed to extend into the ITO pad or expose perimeter seal. Acceptable Quantity N≤2.	X	Y	Z	≤3.0	≤S	≤T	Minor
		X	Y	Z					
≤3.0	≤S	≤T							
2) Chip on the edge of glass  <table><tr><td>X</td><td>Y</td><td>Z</td></tr></table>	X	Y	Z	Minor					
X	Y	Z							

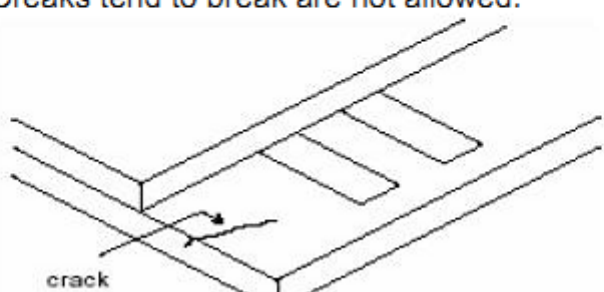
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		Ignore	≤ 0.5	$\leq T$	
		Acceptable Quantity: $N \leq 2$			
		3) Crack Cracks tend to break are not allowed.			Minor
					

- END -